WHAT IS CLAIMED IS:

1. An SRAM-compatible memory device including DRAM cells arranged in a matrix form defined by rows and columns, and externally interfacing with an external system in which no timing period is provided for performing a refresh operation of the DRAM cells, the SRAM-compatible memory device comprising:

first and second memory blocks each having the DRAM cells;

first data lines for transferring data fetched from or to be written in a DRAM cell in the first memory block;

second data lines for transferring data fetched from or to be written in a DRAM cell in the second memory block;

a first sense amplifier for amplifying and latching data in the first data lines;

a second sense amplifier for amplifying and latching data in the second data lines;

a third sense amplifier for amplifying and latching data provided via the first data lines or the second data lines;

a first switching unit for controlling an electrical connection between the first data lines and the third sense amplifier; and

a second switching unit for controlling an electrical connection between the second data lines and the third sense amplifier.

2. The SRAM-compatible memory device according to claim 1, further comprising:

a first equalizing unit for equalizing the first data lines; and

a second equalizing unit for equalizing the second data lines.

3. The SRAM-compatible memory device according to claim 1, wherein first and second external access periods are provided for externally accessing the SRAM-compatible memory device, the first external access period including a first refresh period and a first internal access period and the second external access period including a second refresh period, wherein the SRAM-compatible memory device performs an operation of fetching data from a DRAM cell to be refreshed during the first refresh period, and performs an operation of rewriting the data fetched during the first refresh period in the refreshed DRAM cell during the second refresh period.

4. The SRAM-compatible memory device according to claim 3, wherein the first switching unit is controlled to connect the first data lines to the third sense amplifier during the first refresh period.

5. The SRAM-compatible memory device according to claim 4, wherein the first switching unit is controlled to disconnect the first data lines from the third sense amplifier during the first internal access period.